USER MANUAL

Accessory 70E

TAMAGAWA Encoder Interface Board

300-603692-xUxx

April 15, 2004

DELTA TAU
Data Systems, Inc.
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INTRODUCTION

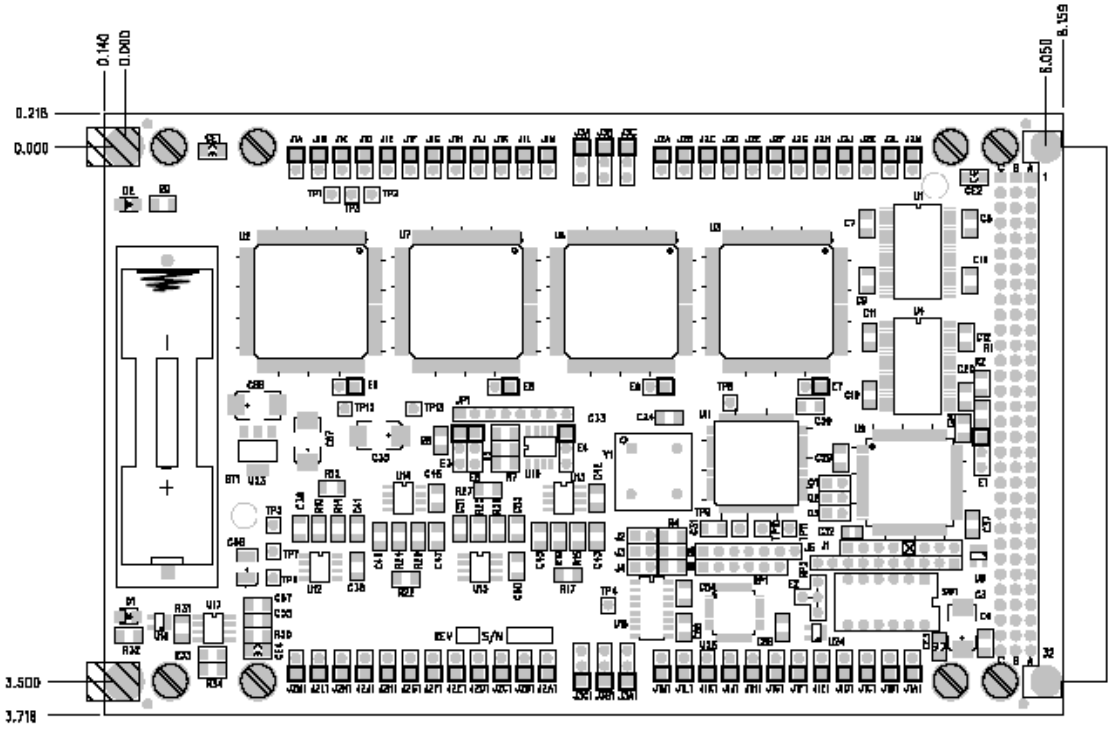
The TAMAGAWA interface card ACC-70E is a UMAC accessory card that connects to the UMAC CPU via a UBUS. The card is designed to handle two or four channels (add Option1).

The Tamagawa interface protocol is a 2.5Mbps RS485 multi-drop style protocol that is designed to receive data serially from an encoder device. It supports encoders that return 17 bits of position data, 16 bits of multi-turn data and 8 bits of alarm data when Data ID3 data code is requested.

This interface accessory card operates with FA-CODER TS5667N420-SA48 and FA-CODER TS5667N120-SA35.

Addressability of the ACC-70E Tamagawa interface allows up to 16 cards (64 encoder channels) to be placed in the UMAC rack.

Layout Diagram



ACC-70E SETUP

PMAC – TAMAGAWA Encoder Data Address Select

Set up the address select sip switch S1

PMAC Chip Select Used	Tamagawa Encoder Data Address	Dip Switch SW1 Position					
		6	5	4	3	2	1
CS10	Y:$78C00-07	**Closed**	Closed	Closed	Closed	Closed	Closed
	Y:$79C00-07	Closed	Closed	Closed	**Open**	Closed	Closed
	Y:$7AC00-07	Closed	Closed	**Open**	Closed	Closed	Closed
	Y:$7BC00-07	Closed	Closed	**Open**	**Open**	Closed	Closed
CS12	Y:$78D00-07	Closed	Closed	Closed	Closed	Closed	**Open**
	Y:$79D00-07	Closed	Closed	Closed	**Open**	Closed	**Open**
	Y:$7AD00-07	Closed	Closed	**Open**	Closed	Closed	**Open**
	Y:$7BD00-07	Closed	Closed	**Open**	**Open**	Closed	**Open**
CS14	Y:$78E00-07	Closed	Closed	Closed	Closed	**Open**	Closed
	Y:$79E00-07	Closed	Closed	Closed	**Open**	**Open**	Closed
	Y:$7AE00-07	Closed	Closed	**Open**	Closed	**Open**	Closed
	Y:$7BE00-07	Closed	Closed	**Open**	**Open**	**Open**	Closed
CS16	Y:$78F00-07	Closed	Closed	Closed	Closed	**Open**	**Open**
	Y:$79F00-07	Closed	Closed	Closed	**Open**	**Open**	**Open**
	Y:$7AF00-07	Closed	Closed	**Open**	Closed	**Open**	**Open**
	Y:$7BF00-07	Closed	Closed	**Open**	**Open**	**Open**	**Open**

Offset Register Mapping Definitions

Address		X –Memory	Y-Memory
Base + 00h	1st Channel		Single turn data and alarms
Base + 01h			Multi turn data and alarms
Base + 02h	2nd Channel		Single turn data and alarms
Base + 03h			Multi turn data and alarms
Base + 04h	3rd Channel		Single turn data and alarms
Base + 05h			Multi turn data and alarms
Base + 06h	4th Channel		Single turn data and alarms
Base + 07h			Multi turn data and alarms

ENCODER CONVERSION TABLE SETUP

Use the previous table and SW1 to select the address. Once the address is selected via the SW1, the corresponding address is used to read the encoder position data.

Example: On all closed positions, the encoder conversion table entry will be:

```
Set:    I8000 = $678C00      ; Y:$3501
        I8001 = $11000       ; Y:$3502

        I8002 = $678C02      ; Y:$3503
        I8003 = $11000       ; Y:$3504

        I8004 = $678C04      ; Y:$3505
        I8005 = $11000       ; Y:$3506

        I8006 = $678C06      ; Y:$3507
        I8007 = $11000       ; Y:$3508
```

Note:

This is a two-line input for one encoder channel. Make sure the related I-Variable (Ix03, Ix04) is pointed to the address of the second line. For example, for the above set up:

I103 and I104 should be = $3502.
I203 and I204 should be = $3504.
I303 and I304 should be = $3506.
I403 and I404 should be = $3508.

Combine Single-Turn and Multi-Turn Data

The Tamagawa absolute encoder has two types of data—single-turn and multi-turn.

A PMAC PLC program is used to combine the data and then copy it to an actual position register.

Warning:

If the actual position is changed while the motors are enabled, a runaway condition may occur which can cause machine damage or bodily injury.

When changing the actual position register using a PLC program, make sure that the motors are not enabled.

Sample PLC Program for Initialize Position

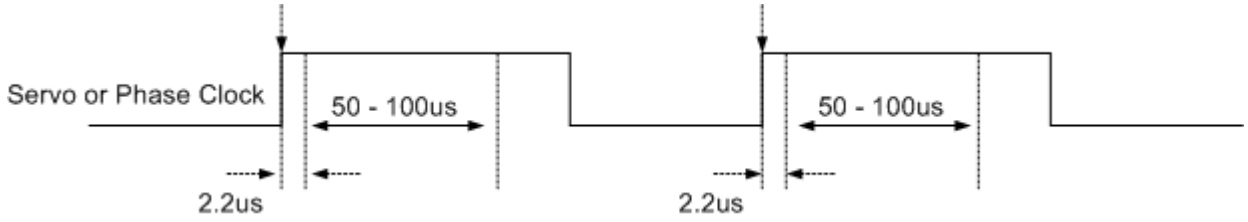
```
M138->X:$B0,18,1                ;#1 Open loop mode bit
M162->D:$8B                     ;#1 Actual position(1/[Ixx08*32])
M110->Y:$78C00,0,20,U           ;ENC1 Single turn data
M111->Y:$78C01,0,16,S           ;ENC1 Multi turn data

M238->X:$130,18,1               ;#2 Open loop mode bit
M262->D:$10B                    ;#2 Actual position(1/[Ixx08*32])
M210->Y:$78C02,0,20,U           ;ENC2 Single turn data
M211->Y:$78C03,0,16,S           ;ENC2 Multi turn data

OPEN PLC2 CLEAR                 ;POS initialize PLC
IF(M138=1 AND M238=1)           ;Make sure if motor is open loop
   P162=M111*131072             ;Convert Multi turn data for to cts for ENC1
   P262=M211*131072             ;Convert Multi turn data for to cts for ENC2
   M162=(P162+M110)*(I108*32)   ;Combine Multi turn and single turn for ENC1
   M262=(P262+M210)*(I208*32)   ;Combine Multi turn and single turn for ENC2
   DIS PLC2                     ;Disable PLC
ENDIF
CLOSE
```

SERVO/PHASE CLOCK SELECTION

Jumper E2 selects the servo or phase clock as the encoder request clock signal. With I-Variable setup such as I7m00, I7m01 and I7m02, clock frequency can be adjusted. Default servo clock frequency is 2.25kHz(442 us) and default phase clock frequency is 9.0khz(110us). Refer to the Turbo PMAC Software Reference manual on how to set up the servo or phase clock.

ACC-70E is responsible for requesting and converting data from the encoder and the process is synchronized with either the servo or phase clock. The rising edge of the clock will trigger the start of the request. The whole process will take approximately 50us to 100us. Therefore, the positive pulse width of the clock must be set to greater than or equal to 100us in order to guarantee completion.

If the positive pulse width is less than the process time for the Tamagawa encoder, it will send previously requested data.



Within 2.2us after the rising edge, ACC-70E will fetch alarm data from the previous conversion and command the encoder to return position data. It takes 50us - 100us for the encoder to return the new position data.

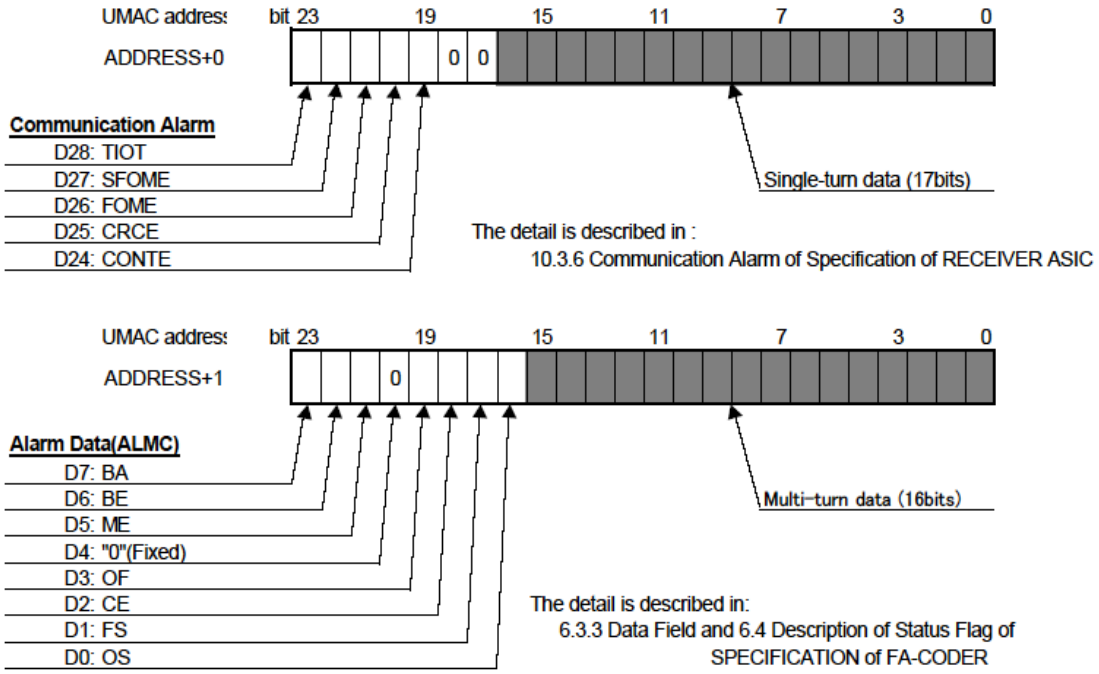
Battery Warning LED

The interface board provides battery back up for the encoder. In addition, it has a battery voltage monitor circuitry that serves as a battery low warning. When the battery voltage drops to 2.3V, the red LED D1 will activate.

Alarm Code

There are bit patterns of alarm code interpreted by the interface card. The following drawing shows the format of those bits.

ALMC bits are data that is returned from encoder register DF7 when DATA ID 3 is requested.



Sample PLC for Alarm

```
M112->Y:$78C00,16,8,U   ;ENC1 ERR1
M113->Y:$78C01,16,8,U   ;ENC1 ERR2

OPEN PLC3 CLEAR
P111=M113*$100+M112
IF(M113&$1=$1)
      SENDS"ALARM D0 OS"
ENDIF
IF(M113&$2=$2)
      SENDS"ALARM D1 FS"
ENDIF
IF(M113&$4=$4)
      SENDS"ALARM D2 CE"
ENDIF
IF(M113&$8=$8)
      SENDS"ALARM D3 OF"
ENDIF
IF(M113&$20=$20)
      SENDS"ALARM D5 ME"
ENDIF
IF(M113&$40=$40)
      SENDS"ALARM D6 BE"
ENDIF
IF(M113&$80=$80)
      SENDS"ALARM D7 BA"
ENDIF
IF(M112&$8=$8)
      SENDS"ALARM D24 CONTE"
```

```
ENDIF
IF(M112&$10=$10)
      SENDS"ALARM D25 CRCE"
ENDIF
IF(M112&$20=$20)
      SENDS"ALARM D26 FOME"
ENDIF
IF(M112&$40=$40)
      SENDS"ALARM D27 SFOME"
ENDIF
IF(M112&$80=$80)
      SENDS"ALARM D28 TIOT"
ENDIF
I5311=10000*8388608/I10
WHILE(I5311>0)
ENDW
CLOSE
```

RESET ENCODER'S ABSOLUTE POSITION REGISTERS

The absolute and multi-turn data position registers can be reset to zero. When resetting the single-turn resister to zero, only the MSB 11 bits will be cleared. The remaining six LSB bits are not cleared.

When resetting the absolute position registers in the encoder, reset the single-turn data before resetting the multi-turn data.

To reset absolute position, write 00 to the base address 12 times for the single-turn reset. To reset the multi-turn data register, write 00 to the base address +1 (also 12 times).

Sample PLC

```
Y:$78C00          ; Channel#1 single turn data with SW1 default setting.
Y:$78C01          ; Channel#1 multi turn data with SW1 default setting.
Y:$78C02          ; Channel#2 single turn data with SW1 default setting.
Y:$78C03          ; Channel#2 multi turn data with SW1 default setting.
Y:$78C04          ; Channel#3 single turn data with SW1 default setting.
Y:$78C05          ; Channel#3 multi turn data with SW1 default setting.
Y:$78C06          ; Channel#4 single turn data with SW1 default setting.
Y:$78C07          ; Channel#4 multi turn data with SW1 default setting.

OPEN PLC1 CLEAR
      WHILE(P501<12)                ;Execute reset sequence 12 times
          CMD"WY:$78C08,0"          ;Zero reset channel#1 single turn data
          P501=P501+1
      ENDW
      P501=0
      I5111=20*8388608/I10          ;20msec timer
      WHILE(I5111>0)
      ENDW
      WHILE(P501<12)
          CMD"WY:$78C09,0"          ;Zero reset channel#1 multi turn data
          P501=P501+1
      ENDW
      P501=0
      DIS PLC1
CLOSE
```

JUMPER CONFIGURATIONS

E1 Turbo-PMAC/MACRO Select

Position	Setting	Function
E1	1-2 Default	Turbo 3U PMAC CPU
	3-4	Macro 3U CPU

E2 SYNC Clock Select

Position	Setting	Function
E2	1-2	Use phase clock as encoder request signal
	2-3 Default	Use servo clock as encoder request signal

E6-E9 Request Signal Enable/Disable Select

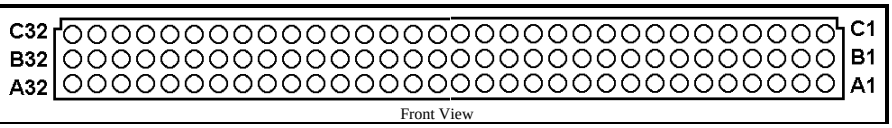
Position	Setting	Function
E6	On Default	Enable request signal for Channel 1
	Off	Disable request signal for Channel 1
E7	On Default	Enable request signal for Channel 2
	Off	Disable request signal for Channel 2
E8	On Default	Enable request signal for Channel 3
	Off	Disable request signal for Channel 3
E9	On Default	Enable request signal for Channel 4
	Off	Disable request signal for Channel 4

J10 Modified SYNC Pulse

Position	Setting	Function
J10	On	Enable modified sync pulse
	Off Default	Disable modified sync pulse

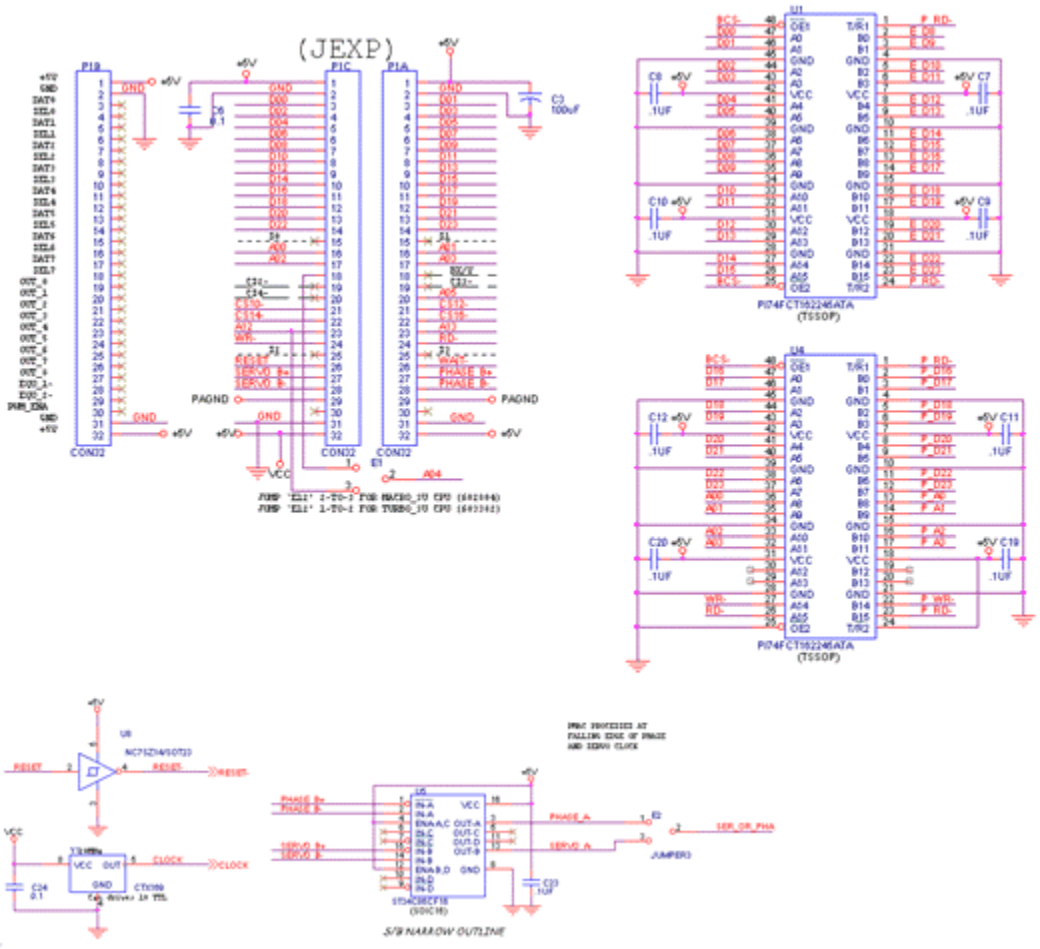
JEXP Pinouts

P1 JEXP (96-Pin Header)



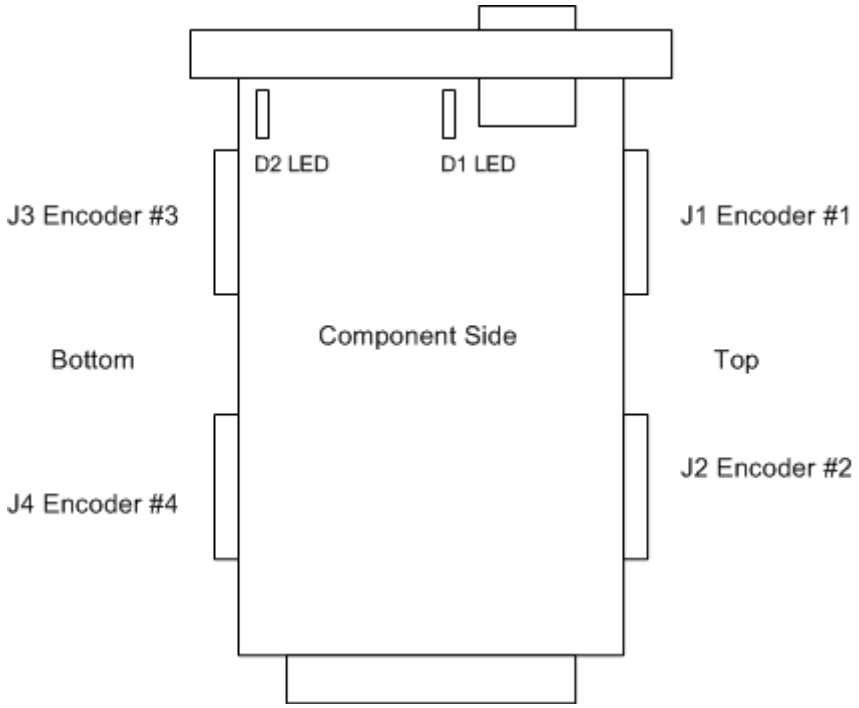
Pin #	Row A	Row B	Row C
1	+5Vdc	+5Vdc	+5Vdc
2	GND	GND	GND
3	BD01	DAT0	BD00
4	BD03	SEL0	BD02
5	BD05	DAT1	BD04
6	BD07	SEL1	BD06
7	BD09	DAT2	BD08
8	BD11	SEL2	BD10
9	BD13	DAT3	BD12
10	BD15	SEL3	BD14
11	BD17	DAT4	BD16
12	BD19	SEL4	BD18
13	BD21	DAT5	BD20
14	BD23	SEL5	BD22
15	BS1	DAT6	BS0
16	BA01	SEL6	BA00
17	BA03	DAT7	BA02
18	BX/Y	SEL7	BA04
19	CS3-	BA06	CS2-
20	BA05	BA07	CS4-
21	CS12-	BA08	CS10-
22	CS16-	BA09	CS14-
23	BA13	BA10	BA12
24	BRD-	BA11	BWR-
25	BS3	MEMCS0-	BS2
26	WAIT-	MEMCS1-	RESET
27	PHASE+	IREQ1-	SERVO+
28	PHASE-	IREQ2-	SERVO-
29	ANALOG	GND IREQ3-	ANALOG GND
30	-15Vdc	PWRGND	+15Vdc
31	GND	GND	GND
32	+5Vdc	+5Vdc	+5Vdc
For more details about the JEXP, see the UBUS Specification Document.			

JEXP Layout Diagram



CONNECTOR PINOUTS

The DB15 style connectors on the ACC-70E are described as J1 Top, J2 Top, J1 Bottom and J2 Bottom. The top connectors have the encoder signals for encoders 1 and 4 and the bottom connectors have the encoder signals for encoders 2 and 3.



Connector J1 – Encoder 1

Pin#	Symbol	Function	Description
1	GND	Reference	+5V and battery return
2	DATA +	Input	Encoder data +
3	CLOCK -	Output	Encoder request signal clock out +
4	+5V	Output	
5	BATTERY +	Output	3.6V battery voltage out
6		N/A	
7	CASE GND	Chassis	
8	CASE GND	Chassis	
9	GND	Reference	+5V and battery return
10	DATA -	Input	Encoder data -
11	CLOCK +	Output	Encoder request signal clock out -
12	+5V	Output	
13		N/A	
14		N/A	
15	CASE GND	Chassis	

Connector J2 – Encoder 2

Pin#	Symbol	Function	Description
1	GND	Reference	+5V and battery return
2	DATA +	Input	Encoder data +
3	CLOCK -	Output	Encoder request signal clock out +
4	+5V	Output	
5	BATTERY +	Output	3.6V battery voltage out
6		N/A	
7	CASE GND	Chassis	
8	CASE GND	Chassis	
9	GND	Reference	+5V and battery return
10	DATA -	Input	Encoder data -
11	CLOCK +	Output	Encoder request signal clock out -
12	+5V	Output	
13		N/A	
14		N/A	
15	CASE GND	Chassis	

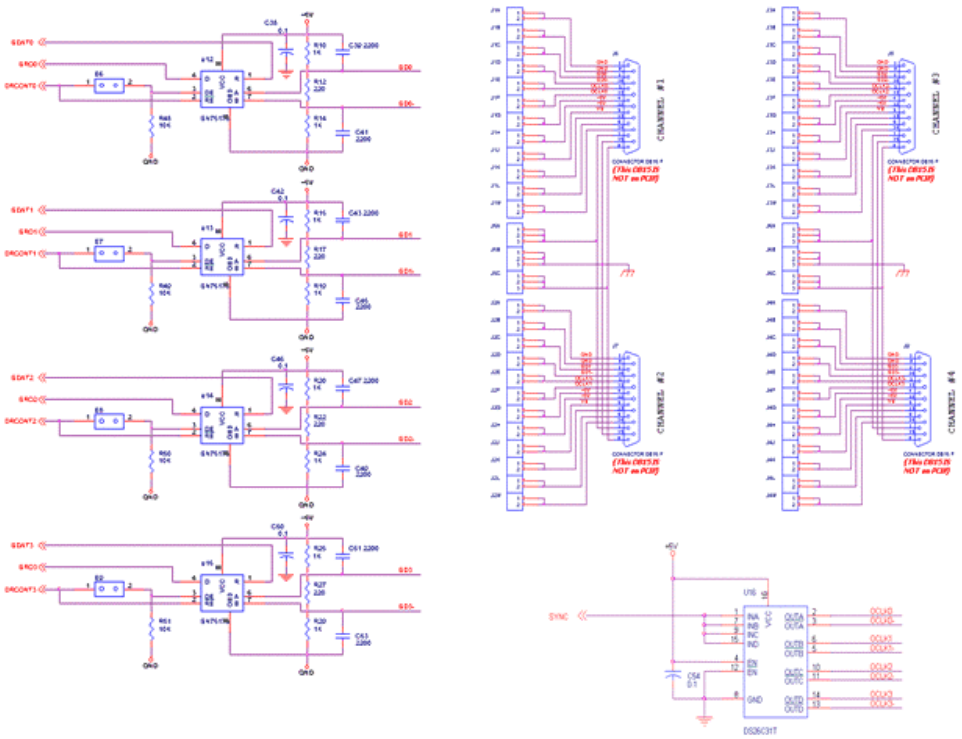
Connector J3 – Encoder 3

Pin#	Symbol	Function	Description
1	GND	Reference	+5V and battery return
2	DATA +	Input	Encoder data +
3	CLOCK -	Output	Encoder request signal clock out +
4	+5V	Output	
5	BATTERY +	Output	3.6V battery voltage out
6		N/A	
7	CASE GND	Chassis	
8	CASE GND	Chassis	
9	GND	Reference	+5V and battery return
10	DATA -	Input	Encoder data -
11	CLOCK +	Output	Encoder request signal clock out -
12	+5V	Output	
13		N/A	
14		N/A	
15	CASE GND	Chassis	

Connector J4 – Encoder 4

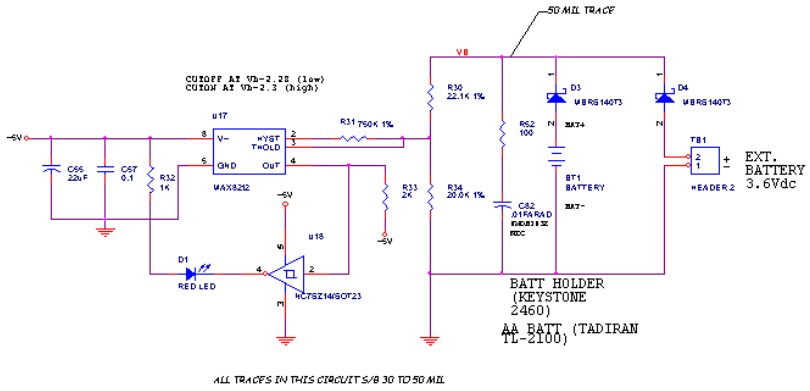
Pin#	Symbol	Function	Description
1	GND	Reference	+5V and battery return
2	DATA +	Input	Encoder data +
3	CLOCK -	Output	Encoder request signal clock out +
4	+5V	Output	
5	BATTERY +	Output	3.6V battery voltage out
6		N/A	
7	CASE GND	Chassis	
8	CASE GND	Chassis	
9	GND	Reference	+5V and battery return
10	DATA -	Input	Encoder data -
11	CLOCK +	Output	Encoder request signal clock out -
12	+5V	Output	
13		N/A	
14		N/A	
15	CASE GND	Chassis	

Connector Layout Diagram



TB1 – External Power Supply

Pin #	Signal Description	Note
1	-BATT	For external power supply
2	+BATT	For external power supply



LED

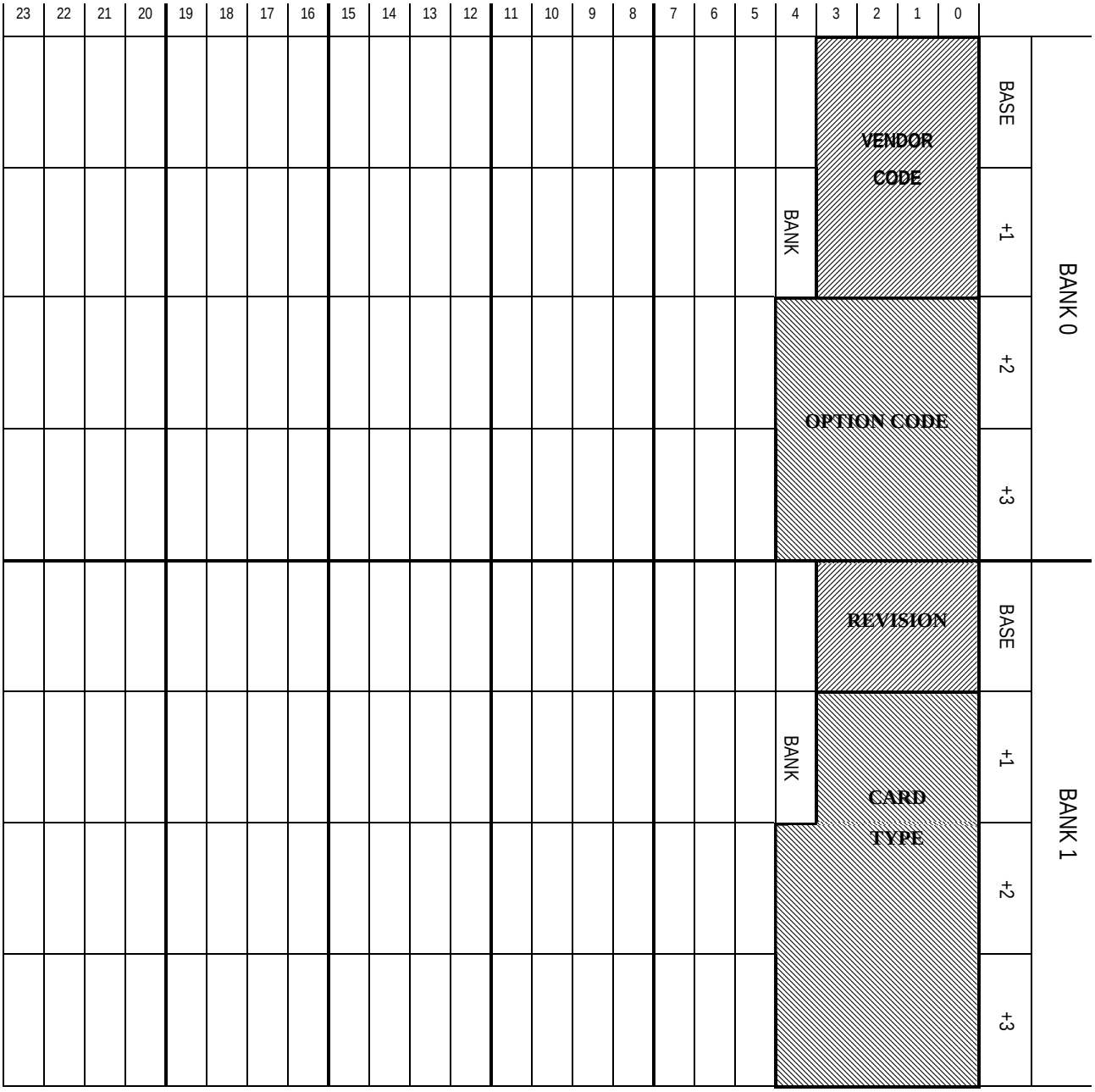
Name	Description	Color	Note
D1	Battery low	RED	Turn off normally
D2	Power good	RED	Turn on normally

BOARD CONFIGURATION MEMORY MAP

The board configuration memory mapping for Turbo UMAC models contains data pertaining to the configuration of products that are plugged into the UBUS backplane.

On power-up or at any time, the UBUS processor (normally a Turbo UMAC processor) is capable of polling this block of memory to establish the mapping of hardware.

Each block of memory contains four address locations that may be polled. There are two banks of four address locations that may be selected so that the processor can read data from up to eight address locations.



Bank
Place a 0 into this bit to select Bank 0. Place a 1 into this bit to select Bank 1.

Vendor Code
Delta Tau Data Systems, Inc. products will have a 1 in this 4-bit address field. Products from other companies will have other values returned in this field.

Option Code
This 5-bit field contains data that pertains to options that are installed on the accessory card. Each product will have a different meaning to the data in this field.

Revision
This 4-bit field indicates the revision level of the board assembly. Usually, this value is hard coded in the circuitry of the board fabrication.

Card Type
This 14-bit address field contains information pertaining to a part number assigned to the board. Usually, this value relates to a vendor's board assembly part number. Delta Tau Data Systems, Inc. uses their 6-digit part number converted to hexadecimal in this field.

Option Codes
The CS10, CS12, CS14 and CS16 selects that are used for the ACC-70E and I/O cards allows for up to 16 board configuration slots to be used. The dip switch selects between any of the 16 banks of memory. This allows up to 16 ACC-70Es to be logically configured.